MEMORIES HAVING REDUCED BITLINE VOLTAGE OFFSETS

ABSTRACT OF THE DISCLOSURE

A memory device design is provided. The memory device includes a memory core having a depth that defines a plurality of words, and a word width that is defined by multiple pairs of a global bitline and a global complementary bitline. The memory device further includes a core cell having a bitline and a complementary bitline, and a flipped core cell that has a flipped bitline and a flipped complementary bitline. The multiple pairs of the global bitline and the global complementary bitline have a plurality of core cells that are defined by alternating ones of the core cell and the flipped core.